(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : 0 454 440 A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number : 91303688.5

(22) Date of filing : 24.04.91

(51) Int. Cl.^{5} : H01L 23/495, H01L 21/56, B29C 45/14

(30) Priority : 25.04.90 JP 109934/90

(43) Date of publication of application :
30.10.91 Bulletin 91/44

(84) Designated Contracting States :
DE FR GB

(71) Applicant : SONY CORPORATION
7-35, Kitashinagawa 6-chome Shinagawa-ku
Tokyo (JP)

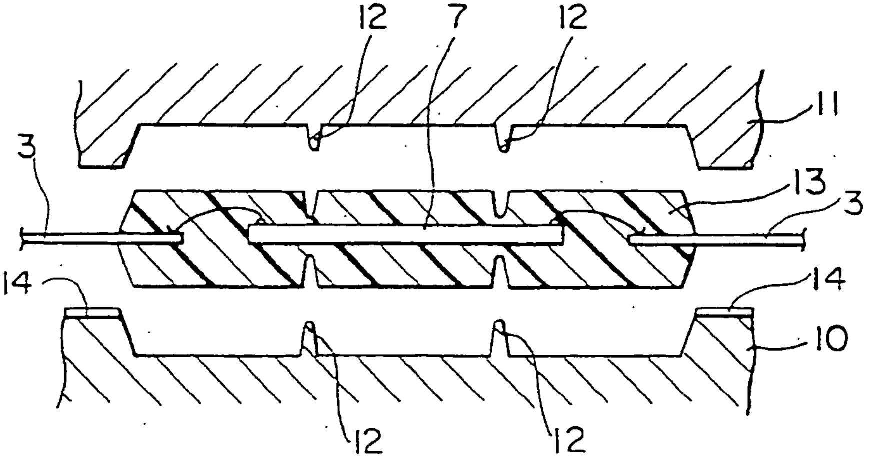
(72) Inventor : Asami, Yukio, c/o Sony Corporation
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)
Inventor : Fukazawa, Hiroyuki, c/o Sony Corporation
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)
Inventor : Kojima, Akira, c/o Sony Corporation
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)

(74) Representative : Targett, Kenneth Stanley et al
D. Young & Co. 10 Staple Inn
London WC1V 7RD (GB)

(54) Packaging of semiconductor chips.

(57) A semiconductor device is fabricated by placing a semiconductor chip (7) in a lead frame which has no die pad. Electrodes of the chip are connected by bonding wires to respective lead fingers (3). Additionally, the lead frame has movement restricting fingers which limit horizontal movement of the chip within the lead frame during injection of resin into a mould surrounding the chip. Furthermore, the mould has horizontal movement restricting projections (12) to limit vertical movement of the chip within the mould cavity. The restriction on horizontal and vertical movement of the chip reduces the risk of the bonding wires being broken or short circuited during the resin injection process.

FIG.3



EP 0 454 440 A1

Jouve, 18, rue Saint-Denis, 75001 PARIS

This invention relates to packaging of semiconductor chips, and in particular various aspects of the present invention relate to a packaged semiconductor device, a combination of a semiconductor chip and a lead frame therefor, a method of manufacturing a semiconductor device, and a mould for moulding a resin package around an assembly of a semiconductor chip and a plurality of lead fingers.

There are a number of known manners of manufacturing a semiconductor device, in which a semiconductor chip is sealed in a resin package. Figure 4 of the accompanying drawings shows a known "die pad" construction in which a chip c is bonded to a die-pad a by a bonding material d, such as a silver paste or a gold-silicon eutectic alloy. The die-pad a is connected to a peripheral portion of a lead frame by connecting fingers a'. A plurality of lead fingers b project from the peripheral portion of the lead frame, and each lead finger b is connected to a respective electrode of the chip c by a respective bonding wire e. The chip c, die-pad a, bonding wires e and inner ends of the fingers a', b are then placed in a moulding die and sealed in a resin package.

Another known "chip-on-lead" type of construction is shown in Figure 5. In this case, an insulator f, such as a polyimide sheet, is placed on the inner ends of lead fingers b, a semiconductor chip c is placed on the insulator f and the electrodes of the semiconductor chip c are connected to respective inner ends of the lead fingers b by respective bonding wires e. Again, the assembly is then sealed in a resin package.

A further known "lead-on-chip" type of construction is shown in Figure 6. In this case, a surface of a semiconductor chip c, excluding the electrodes thereon, is covered with an insulator f, lead fingers b are placed on the insulator f, and the lead fingers b are connected to respective electrodes by respective bonding wires e. Once again, the assembly is then sealed in a resin package.

Lastly, Figure 7 shows a known "directly connected" form of construction, in which electrode pads g of a semiconductor chip c project upwardly from the upper surface of the chip c, and the inner ends of lead fingers b are directly connected to the electrode pads g. The assembly is then sealed in a resin package.

It is desirable that the height of the semiconductor device is as small as possible. However, in the die pad construction described above, the thickness of the die pad a and bonding material d add to the height of the package. In the chip-on-lead and lead-on-chip forms of construction described above, the thickness of the insulators f and the lead fingers b add to the height of the package. In the directly connected form of construction described above, the thickness of the lead fingers b and the height of the electrode pads g add to the overall height of the semiconductor package. Also, the die pad construction suffers from the problem that thermal stress is induced in the device due to differences in the coefficients of thermal expansion of the die pad a, the semiconductor chip c and the resin of the package, which can cause a breakdown in bonding between the chip c and the die pad a, between the die pad a and the resin package, or between the chip c and the resin package.

The problems with which various aspects of the present invention are concerned are: to enable a semiconductor device to be produced which has a decreased height; to alleviate thermal stresses in the semiconductor package; and/or to enable the semiconductor device to be produced reliably, such that there is a small risk of the bonding wires being broken or short circuited while the resin package is being formed around the assembly of the chip, bonding wires and lead fingers.

In accordance with one aspect of the present invention, there is provided a semiconductor device, in which the inner ends of the lead fingers lie between the planes of the upper and lower surfaces of the semiconductor chip, and the resin package directly contacts both the upper surface and the lower surface of the chip. Thus, a reduce height package is provided, and no thermal stress is induced due to the presence of a die pad.

The lead fingers may be provided by portions of a lead frame, and preferably additional finger portions are provided which do not normally contact the chip, but which restrict lateral movement of the chip with respect to the lead frame during moulding of the resin package around the assembly.

In accordance with another aspect of the present invention, there is provided a mould for moulding a resin package around an assembly comprising a semiconductor chip having a plurality of electrodes, a plurality of lead fingers projecting away from the chip, and a plurality of bonding wires each connecting a respective one of the electrodes to a respective one of the lead fingers. The mould comprises first and second complementary mould parts. At least one projection projects from at least one of the mould parts interiorly of the mould cavity provided by the mould parts for restricting movement of the chip in the mould cavity when resin is injected into the mould cavity.

Other features of the present invention are defined in the accompanying claims.

There follows a description of a preferred embodiment and example of the present invention with reference to the accompanying drawings, in which:

Fig. 1 is a partial perspective view of a lead frame to which are connected a pair of semiconductor chips;

Fig. 2 is a sectional view of a moulding die loaded with a lead frame and a semiconductor chip;

Fig. 3 is a sectional view of a resin package as formed by the moulding die of Fig. 2;

Fig. 4 is a sectional view of a known die pad form of assembly of a lead frame and semiconductor chip;

Fig. 5 is a perspective view of a known chip-on-lead form of assembly of semiconductor chip and lead frame;

Fig. 6 is a perspective view of a known lead-on-chip form of assembly of a semiconductor chip and lead frame; and

Fig. 7 is a sectional view of a known direct connection form of assembly of a semiconductor chip and lead frame.

Referring to Figures 1 to 3, a lead frame 1 for manufacturing a plurality of semiconductor devices has apertures 2 for receiving semiconductor chips 7 in a longitudinal arrangement at regular intervals. The apertures 2 are provided instead of the die pads in the known die pad form of construction. Each aperture 2 is of a size such that the respective chip 7 could be passed through the aperture.

The lead frame 1 has peripheral frame members 5 surrounding each aperture 2, tie bars 4 connecting portions of the lead frame for each chip, lead fingers 3 projecting towards each aperture 2 and horizontal movement restricting fingers 6 projecting inwardly from the side portions of the frame members 5 towards the apertures 2.

Each semiconductor chip 7 is placed in the respective aperture 2. The size of the aperture 2 (defined by inner ends of the lead fingers 3 and movement restricting fingers 6) is such that the lead fingers 3 and the movement restricting fingers 6 do not contact the chip 7.

Each chip 7 has a plurality of electrodes 9, and each electrode is connected to the inner end of a respective one of the lead fingers 3 by a respective bonding wire 8. Thus, each semiconductor chip 7 is connected to the lead frame 1 solely by the bonding wires 8.

Then, the lead frame 1, with the chips 7 connected thereto, is placed in a moulding die, as shown in Figure 2. The moulding die comprises a lower die part 10 and a complementary upper die part 11, and the lead fingers and movement restricting fingers pass through channels 14 between the die parts 10,11. Both die parts 10,11 are provided with vertical movement restricting pins 12, which project towards the chip 7, but which are slightly separated from the upper and lower surfaces of the chip 7. After the chip 7 has been placed in the moulding die, supported solely by the lead frame 1 and the bonding wires 8, resin is injected into the mould cavity of the moulding die to seal the semiconductor chip, the bonding wires 8, and the inner ends of the lead fingers 3 within a resin package 13 as shown in Figure 3.

Although the resin has a sufficiently low viscosity in the initial stage of injection of resin into the mould cavity, the resin tends to urge the chip 7 vertically either towards the lower die part 10 or the upper die part 11, due to slight differences in resistance against the flow of the resin between the upper and lower surfaces of the semiconductor chip 7. However, vertical movement of the chip 7 is restricted by the vertical movement restricting projections 12, so that the chip 7 cannot significantly move towards the lower die part 10 or upper die part 11. As injection progresses, the resin becomes distributed uniformly within the mould cavity, and the resin tends to fill the gaps between the tips of the vertical movement restricting projections 12 and the upper and lower surfaces of the chip 7. Once injection of the resin has been completed, the chip 7 tends to return to its original position within the moulding die, and therefore partial exposure of the chip 7 at the locations of the movement restricting projections 12 is unlikely to occur. The viscosity of the resin being injected may also tend to urge the chip sideways in the mould cavity. However, sideways movement of the chip is restricted not only by the bonding wires 8, but also by the horizontal movement restricting fingers 6. Even if the tip of one or more of the horizontal movement restricting fingers 6 possibly remains in contact with a side surface of the chip 7 after the resin has hardened, no problem arises because the portions of the horizontal movement restricting projections which project outside the resin package 13 are subsequently cut off.

After the resin has hardened, the lower and upper die parts 10,11 are separated, and the lead frame with the packages moulded thereon are removed. Then, the horizontal movement restricting portions 6 are cut off flush with the side of each package 13, and the lead fingers 3 are severed each at a location spaced from the resin package so as to form individual connecting leads for the chips.

Claims

1. A semiconductor device, comprising:

a resin package (13);

a semiconductor chip (7) sealed within the package, the chip having upper and lower surfaces lying in upper and lower planes, respectively, and the chip having a plurality of electrodes (9);

a plurality of lead fingers (3) each having an outer end disposed outside the package and each having an inner end disposed within the package and lying between the upper and lower planes; and

a plurality of bonding wires (8) each connecting a respective one of the electrodes to a respective one of the inner ends of the lead fingers;

wherein the resin package directly contacts both the upper surface and the lower surface of the chip.

2. A combination of a semiconductor chip and a lead frame for use in manufacturing a semiconductor device from the chip, the lead frame (1) comprising:

a peripheral portion (5) surrounding a region for receiving the chip; and

a plurality of finger portions (3, 6) projecting from the peripheral portion towards the region and terminating outside the region such that the chip (7) can be disposed in the region without contacting the finger portions and such that the lead frame provides a through aperture in the region for receiving the chip.

3. A combination as claimed in claim 2, wherein the chip has a plurality of electrodes (9), and the plurality of finger portions comprises a plurality of lead finger portions (3) connectable to the electrodes by a plurality of bonding wires (8), and a plurality of movement restricting finger portions (6) for restricting movement of the chip during manufacture of the device.

4. A method of manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip (7), the semiconductor chip having an upper surface and a lower surface and having a plurality of electrodes (9);

providing a lead frame (1), the lead frame comprising a peripheral portion (5) surrounding a region for receiving the chip and a plurality of lead finger portions (3) projecting from the peripheral portion towards the region and terminating outside the region;

placing the chip in the region;

connecting each of the electrodes to a respective one of the lead finger portions with a respective bonding wire (8);

sealing the chip and bonding wires in a resin package (13) such that the lead finger portions project out of the package and such that the resin package directly contacts both the upper surface and the lower surface of the chip; and

severing each of the lead finger portions from the peripheral portion of the frame.

5. A method of manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip (7), the semiconductor chip having a plurality of electrodes (9);

providing a lead frame (1), the lead frame comprising a peripheral portion (5) surrounding a region for receiving the chip and a plurality of lead finger portions (3) projecting from the peripheral portion towards the region and terminating outside the region;

placing the chip in the region;

connecting each of the electrodes to a respective one of the lead finger portions via a respective bonding wire (8) such that the chip is mechanically connected to the peripheral portion solely by the bonding wires and the lead finger portions;

sealing the chip and the bonding wires in a resin package (13) such that the lead finger portions project out of the package; and

severing each of the lead finger portions from the peripheral portion of the frame.

6. A method as claimed in claim 5, wherein the semiconductor chip has an upper surface and a lower surface, and in the sealing step the resin package is caused to contact directly both the upper surface and the lower surface of the chip.

7. A method as claimed in any of claims 4 to 6, wherein the sealing step comprises the steps of:

providing a mould (10, 11) having a wall defining a mould cavity and at least one projection (12) projecting from the wall;

placing the chip and bonding wires in the mould cavity such that the projection does not contact the chip; and

injecting resin into the mould cavity;

whereby the projection restricts movement of the chip in the mould cavity during the injection step.

8. A method as claimed in any of claims 4 to 7, wherein the lead frame has a plurality of movement restricting finger portions (6) projecting from the peripheral portion towards the region, wherein in the connecting step the lead finger portions are connected to the electrodes such that the movement restricting finger portions do not contact the chip, and wherein during the sealing step the movement restricting finger portions restrict movement of the chip in the region.

9. A mould for moulding a resin package around an assembly comprising a semiconductor chip having a plurality of electrodes, a plurality of lead fingers projecting away from the chip, and a plurality of bonding wires each connecting a respective one of the electrodes to a respective one of the lead fingers, the mould comprising first and second complementary mould parts (10, 11) relatively movable into an operative position in which a mould cavity is defined between the mould parts for receiving the chip and bonding wires and a plurality of channels (14) are defined between the mould parts for receiving the lead fingers, and at least one projection (12) projecting from at least one of the mould parts interiorly of the mould cavity for restricting movement of the chip in the mould cavity.

FIG. I

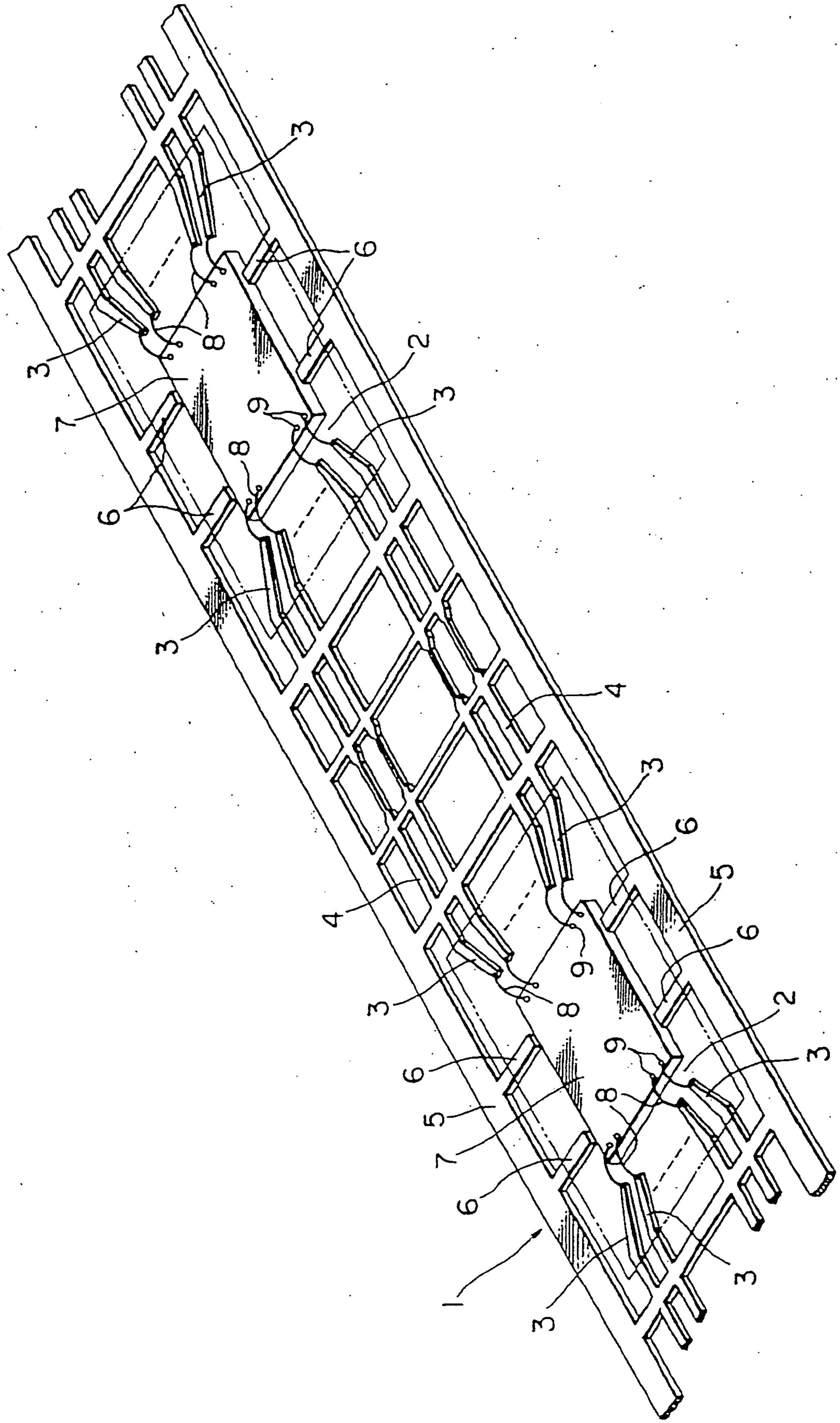


FIG. 2

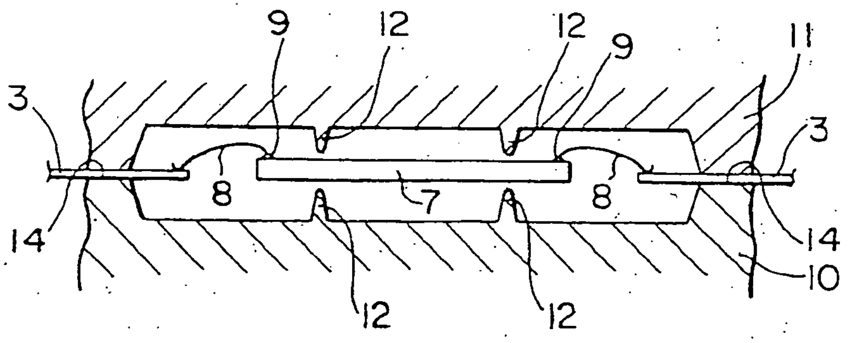


FIG. 3

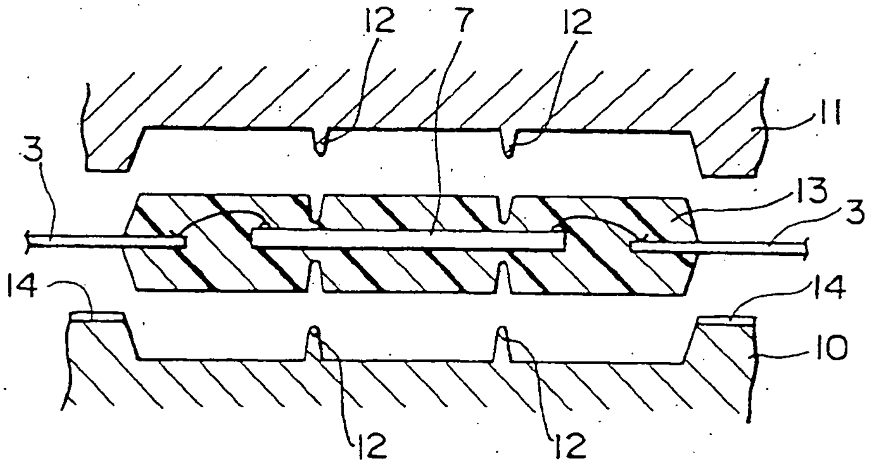


FIG. 4

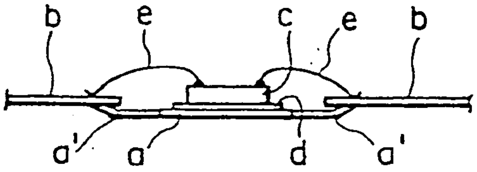


FIG. 5

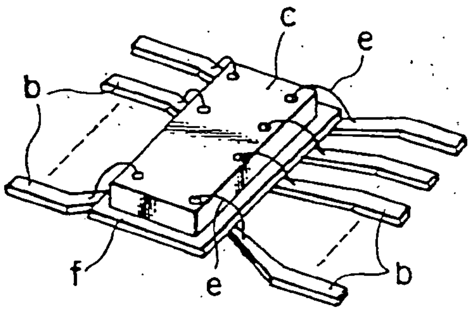


FIG. 6

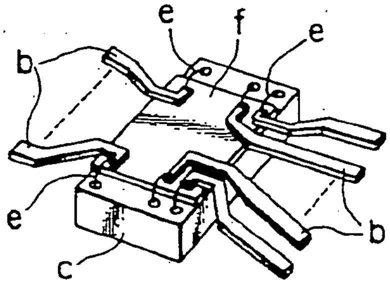
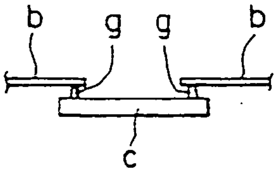


FIG. 7



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 30 3688

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	US-A-4012766 (A.B.PHILLIPS ET AL.) * column 2, line 1 - column 5, line 19; figures 2-7 *	1, 4, 6, 9	H01L23/495 H01L21/56 B29C45/14
X	* ditto *	2, 5	
Y	EP-A-0350833 (FUJITSU LIMITED) * page 8, lines 4 - 8 * * page 8, lines 44 - 48; figures 6h, 11b *	1, 4, 6	
Y	PATENT ABSTRACTS OF JAPAN vol. 14, no. 19 (M-919)(3962) 16 January 1990, & JP-A-01 262115 (SEIKO EPSON CORP) 19 October 1989, * the whole document *	9	
X	EP-A-0273725 (KABUSHIKI KAISHA TOSHIBA) * column 3, lines 2 - 8 * * column 4, lines 11 - 42; figure 8 *	9	
A	* ditto *	7, 8	
P,X	EP-A-0366386 (MOTOROLA,INC) * column 3, line 38 - column 4, line 32; figures 1, 2 *	1-6	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	EP-A-0213764 (THE GENERAL ELECTRIC COMPANY) * column 5, line 57 - column 6, line 43 * * column 8, line 30 - column 9, line 10; figures 2C, 4A-4C *	1, 2, 4, 5	H01L
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 159 (E-326)(1882) 04 July 1985, & JP-A-60 037754 (SUWA SEIKOSHA) 27 February 1985, * the whole document *	1, 2, 4, 5, 9	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	26 JULY 1991	LE MINH, I

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)